

The US Semiconductor Industry's Nanoelectronics Research Initiative: Motivation and Challenges

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In recent generations of CMOS technology, exponentially increasing power density is limiting our ability to reap the historical benefits of continued scaling. Recognizing this challenge, a series of workshops and studies were conducted by groups from US industry (coordinated by the Semiconductor Research Corporation, SRC, and the Semiconductor Industry Association, SIA), academia, and the National Science Foundation (NSF). These studies of fundamental physics considerations indicate that the scaling of devices that use dissipative switching of electron charge as the basis of computation will likely reach a limit within one to two decades. They also resulted in 13 research vectors considered most urgent for finding a replacement switch. In 2005, the SIA chartered the Nanoelectronics Research Initiative (NRI), a joint industry-government program to fund university research, using the top 5 of these research vectors as guiding principles.

NRI Mission: Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe. These devices should show significant advantage over ultimate FETs in power, performance, density, and/or cost to enable the semiconductor industry to extend the historical cost and performance trends for information technology.

In this talk, the scaling challenges facing current CMOS technology will be presented, along with the ultimate limits for charge-switching based devices. The rationale for the 13 research vectors will be discussed, along with the current status of the NRI program.