

Current Trends and Future Directions in Field Effect Transistor Technology

Thomas N. Theis

IBM T.J. Watson Research Center, P.O. Box 218, Yorktown Heights, NY 10598

In a climate of intense economic competition, leading microprocessor manufacturers currently strive to double integration density roughly every two years. At this frantic pace, dimensional tolerances are no longer scaling with dimensions, contributing to growing variability in the properties of nominally identical devices. Innovations in device and circuit co-design are combating this problem to some extent, but economic limits on allowable power dissipation are now severely limiting clock speeds. The introduction of high-dielectric constant gate insulators and the likely introduction of one or more varieties of wrap-around gate devices (tri-gate, fin-FET, or nanowire FETs) will help with power dissipation. Beyond this, researchers are beginning to explore various concepts for improved subthreshold slope FETs. Such devices promise high performance at greatly reduced power consumption. Finally, the Nanoelectronics Research Initiative is funding university research aimed at device concepts that can greatly exceed the ultimate capabilities of the field effect transistor.